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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Jensen**
Application No.	:	**10/052,277**
Filed	:	**01/17/2002**
For	:	**LOW-POWER BUS INTERFACE**

APPEAL BRIEF

On Appeal from Group Art Unit 2112

Date: 05/28/2007

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Michael Ure
(Name)

M Ure 5/29/07
(Signature and Date)

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TABLE OF CASES

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-8, 10-13 and 15-19 are pending, all of which stand finally rejected and form the subject matter of the present appeal. Claims 9 and 14 have been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a low-power bus interface in which a central activity detector detects a data transfer operation and applies an enabling signal to bus interfaces of a plurality of components, the components otherwise being in a low-power

state, to enable the components to receive data as part of the data transfer operation. The activity detector is low-latency, allowing the device to be enabled without delaying the data transfer operation. The invention, with its use of centralized activity detector, is particular well-suited for use in System-on-Chip (SOC) applications (as compared to, for example, board-level applications). As noted at paragraph [0014] of the specification, the invention is based on the observation that, substantial power savings can be achieved by providing a common activity detector that enables each target when activity is detected, rather than continuously monitoring the bus for activity at each target.

Claim 1 relates to such a system. As recited in independent claim 1, a plurality of components each have a bus interface, and a bus structure is configured to facilitate communications among the plurality of components. An activity detector is configured to detect an initiation of a data-transfer operation and to provide therefrom an enabling signal that is communicated to bus interfaces of a plurality of components, wherein the bus interface is configured to be enabled to receive data from the bus structure as part of the data-transfer operation upon receipt of the enabling signal from the activity detector.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A system comprising:	Fig. 1, Fig. 2	
a plurality of components each having a bus interface,	Fig. 1, 110, 120; Fig. 2, 110, 120	Paragraphs [0011]; [0017]
a bus structure is configured to facilitate communications among the plurality of components, and	Fig. 1, 150; Fig. 2, 150	Paragraphs [0010]; [0017]
an activity detector that is configured to detect an initiation of a data-transfer operation and to provide therefrom an enabling signal that is communicated	Fig. 1, 180; Fig. 2, 180	Paragraphs [0012], [0015]; [0022]

to bus interfaces of a plurality of said components,		
wherein the bus interface is configured to be enabled to receive data from the bus structure as part of said data-transfer operation upon receipt of the enabling signal from the activity detector.	Fig. 1; Fig. 2	Paragraphs [0012]; [0022]

Claim 10 relates to a method of reducing power consumption in a system comprising a plurality of components each having bus interfaces that are configured to communicate via a bus structure. As recited in independent claim 10, the method involves detecting an initiation of a data transfer operation by a component of the plurality of components, communicating an enabling signal to more than one other component of the plurality of components, and enabling a bus interface at each of the more than one other components to receive data signals as part of the data transfer operation, based on the enabling signal.

The following analysis of independent claim 10 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
10. A method of reducing power consumption in a system comprising a plurality of components each a having bus interface that are configured to communicate via a bus structure, comprising:	Fig. 1, 110, 120, 150; Fig. 2, 110, 120, 150	Paragraphs [0010], [0011]; [0017]
detecting an initiation of a data transfer operation by a component of the plurality of components,	Fig. 1, 180; Fig. 2, 180	Paragraphs [0012], [0015]; [0022]

communicating an enabling signal to more than one other component of the plurality of components,	Fig. 1, 180; Fig. 2, 180	Paragraphs [0012], [0015]; [0022]
and enabling a bus interface at each of the more than one other components to receive data signals as part of the data transfer operation, based on the enabling signal.	Fig. 1; Fig. 2	Paragraphs [0012]; [0022]

Claim 15 relates to an electronic circuit, such as an integrated circuit, comprising a plurality of initiators that are configured to selectively initiate data-transfer operations via a bus structure, an activity detector that is configured to detect an initiation of a data-transfer operation from any of the plurality of initiators, and to generate therefrom an enabling signal, and a plurality of targets that are configured to process the data-transfer operations. Each of the plurality of targets includes an interface for receiving the data-transfer operations, the interface of each being configured to receive data of the data-transfer operation in dependence upon the enabling signal from the activity detector.

The following analysis of independent claim 15 is presented for convenience:

Element	Figure(s)	
15. An electronic circuit comprising:	Fig. 1, Fig. 2	
a plurality of initiators that are configured to selectively initiate data-transfer operations via a bus structure,	Fig. 1, 110; Fig. 2, 110	Paragraphs [0011]; [0017]
an activity detector that is configured to detect an initiation of a data-transfer operation from any of the plurality of initiators, and to	Fig. 1, 180; Fig. 2, 180	Paragraphs [0012], [0015]; [0022]

generate therefrom an enabling signal,		
and a plurality of targets that are configured to process the data-transfer operations, each of the plurality of targets including an interface for receiving the data-transfer operations,	Fig. 1, 120; Fig. 2, 120	Paragraphs [0011]; [0017]
wherein the interface of each is the plurality of targets is configured to receive data of the data-transfer operations in dependence upon the enabling signal from the activity detector.	Fig. 1; Fig. 2	Paragraphs [0012]; [0022]

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 1-8, 10-13 and 15-19 are anticipated by Mitchell.

VII. ARGUMENT

I. Rejection of Claims 1-8, 10-13 and 15-19 as Being Anticipated by Mitchell

The technical approach and technical context of Mitchell differs substantially from the present invention. These differences are reflected in various ways in independent claims 1, 10 and 15. In particular, whereas the present invention is particularly suited for SOCs, Mitchell is directed toward a board-level bus system. In the case of the present invention, a common activity detector is provided that enables each target when activity is detected. In Mitchell, the bus is continually monitored for activity at each target.

Referring to Figures 3 and 16 of Mitchell, each subsystem 1-n is provided with a bus interface 54a-n that performs the steps of Figure 16. Namely, each bus interface receives over the bus an address for the current bus cycle, decodes the address, and compares the decoded address with the address of the subsystem. If the addresses are equal, then the bus interface provides a bus clock signal to the core logic of the subsystem during the bus cycle. If not, the bus interface withholds the bus clock from the core logic of the subsystem during the bus cycle.

It will be appreciated that Mitchell does not teach or suggest various features of claim 1, including "*an enabling signal* (singular) that is communicated to *bus interfaces* (plural) of a plurality of components". Rather, Mitchell teaches bus interfaces of each of plurality of components *each providing its own separate enabling signal.* That enabling signal (sel1-n) is communicated *only to its own bus interface* (i.e., clock gate logic 53a-n).

It will further be appreciated that Mitchell does not teach or suggest various features of claim 10, including "communicating *an enabling signal* to *more than one other components* of the plurality of components, and *enabling a bus interface at each* of the more than one other components to receive data signals as part of the data transfer operation, based on the enabling signal." Rather, Mitchell teaches communicating an enabling signal only within a single component, and enabling the bus interface at that component only.

Finally, it will be appreciated that Mitchell does not teach or suggest various features of claim 15, including "an activity detector that is configured to detect an initiation of a data-transfer operation from any of the plurality of initiators, and to generate therefrom *an enabling signal,*...wherein the interface of *each of the plurality of targets* is configured to receive data of the data-transfer operations in dependence upon *the enabling signal* from the activity detector." Rather, Mitchell teaches each of a plurality of targets being configured to receive data in dependence upon its own enabling signal.

It may be seen therefore that Mitchell does *not* anticipate claim 1, claim 10 or claim 15.

With regard to dependent claims 2-8, 11-13 and 16-19, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claims.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 05/27/2007

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A system comprising: a plurality of components, a bus structure that is configured to facilitate communications among the plurality of components, and an activity detector that is configured to detect an initiation of a data-transfer operation and to provide therefrom an enabling signal that is communicated to bus interfaces of a plurality of said components, wherein the bus interface is configured to be enabled to receive data from the bus structure as part of said data-transfer operation upon receipt of the enabling signal from the activity detector.

2. The system of claim 1, wherein the activity detector is further configured to detect a completion of the data-transfer operation, and terminates the enabling signal based on the completion of the data-transfer operation, and the bus interface is configured to be disabled from receiving data from the bus structure upon termination of the enabling signal.

3. The system of claim 1, wherein the enabling signal includes a gated clock signal.

5. The system of claim 1, wherein the activity detector includes: a set-reset device that is set upon detection of the initiation of the data-transfer operation, and a delay device, operably coupled to the set-reset device, that is configured to provide the enabling signal synchronous with a system clock that is common to the bus structure, based on whether the set-reset device is set.

6. The system of claim 5, wherein the set-reset device is reset upon detection of a completion of the data-transfer operation.

7. The system of claim 1, further including a bus controller that is configured to establish a communications path between an initiating component of the plurality of components and a target component of the plurality of components, wherein the activity detector provides the enabling signal within a time duration consumed by the bus controller to establish the communications path.

8. The system of claim 7, wherein the bus controller includes one or more devices that operate in dependence upon the enabling signal.

10. A method of reducing power consumption in a system comprising a plurality of components that are configured to communicate via a bus structure, comprising: detecting an initiation of a data transfer operation by a component of the plurality of components, communicating an enabling signal to more than one other components of the plurality of components, and enabling a bus interface at each of the more than one other components to receive data signals as part of the data transfer operation, based on the enabling signal.

11. The method of claim 10, further including detecting a completion of the bus activity, and disabling the bus interface at each of more than one other components, based on the

completion of the bus activity.

12. The method of claim 10, further including synchronizing the enabling signal to a system clock that is common to the bus structure.

13. The method of claim 10, further including establishing a communications path between the component that initiated the bus activity and a target component of the more than one other components, and enabling the bus interface at the target component within a time duration required to establish the communications path.

15. An electronic circuit comprising: a plurality of initiators that are configured to selectively initiate data-transfer operations via a bus structure, an activity detector that is configured to detect an initiation of a data-transfer operation from any of the plurality of initiators, and to generate therefrom an enabling signal, and a plurality of targets that are configured to process the data-transfer operations, each of the plurality of targets including an interface for receiving the data-transfer operations, wherein the interface of each of the plurality of targets is configured to receive data of the data-transfer operations in dependence upon the enabling signal from the activity detector.

16. The electronic circuit of claim 15, wherein the plurality of initiators are configured to effect the data-transfer operations at a system clock speed, and the interface of each of the plurality of targets is configured to operate at the system clock speed only when the activity detector provides the enabling signal.

17. The electronic circuit of claim 16, wherein the enabling signal includes a clocking signal that operates at the system clock speed.

18. The electronic circuit of claim 15, wherein the activity detector is further configured to detect the completion of the data-transfer operations, and to terminate the generation of the enabling signal based on a completion of the data-transfer operations.

19. The electronic circuit of claim 15, further including a bus controller that is configured to establish a communications path between an initiator of the plurality of initiators and a target of the plurality of targets, wherein the activity detector is configured to generate the enabling signal within a time duration required by the bus controller to establish the communications path.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE